Simulation of Self-Heating Effect in SOI nMOSFETs

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***Abstract*— Silicon-On-Insulator (SOI) transistors have major advantages compared to conventional MOS devices due to improvements in electrical characteristics and suppression of undesirable effects. However, the heat generated by current flow faces finds a barrier to its dissipation in the buried oxide due to the low thermal conductivity in relation to the silicon. The temperature rise is higher in the channel region, so the mobility of the electrons is degraded, causing a decrease in the drain current. Low temperature operation is known to improved MOSFET performance, increasing drain current, and hence, heating. In this work, numerical simulation have been performed, considering lattice heating in order to analyze the occurrence of self-heating effect and the impact of temperature over this effect.**

Keywords*— *MOS Transistors, SOI Technology, Self-heating, Electrical Characterization, Numerical Simulation.

I. INTRODUCTION

The Silicon-On-Insulator (SOI) transistor, presented in Fig. 1, has a great integration capability, when compared to the conventional MOS transistor. There are some notable advantages provided by this device, such as increased mobility, transconductance [1], decrease of parasitic capacitances and suppression of the thyristor effect. However, the buried oxide makes it difficult to dissipate heat generated by the conduction process of the drain current, degrading the mobility of the carriers and thus causing changes in the electrical characteristics of the device [2].

Self-heating in the channel region due to undissolved power degrades the mobility of the carriers and consequently there is a reduction of the drain current in the saturation region as schematically represented in in Fig. 2 [3]. As the devices become smaller and thinner, self-heating becomes more pronounced. Thus, the heat path between the source/drain decreases, the thermal resistance between them is higher and thus the temperature of the transistor body increases [4].

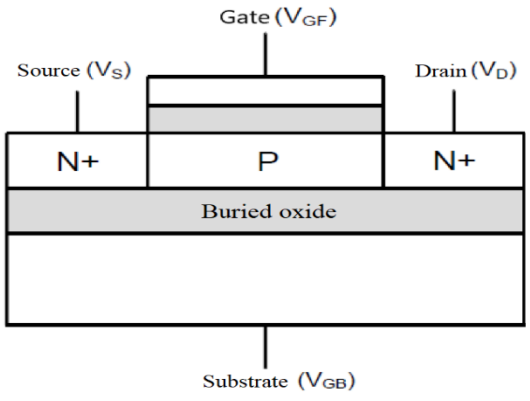

Fig. 1- Longitudinal section of a SOI nMOSFET.

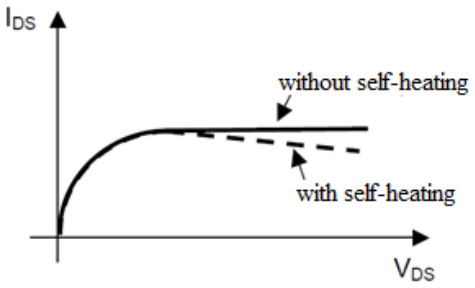

Fig. 2 - Schematic curve indicating the occurrence of self-heating effect.

An explanation for the difficulty of thermal conduction by buried oxide is due to the amorphous structure of the arrangement of the atoms as presented in Fig. 3, making the thermal characteristics of the oxide inferior than in the silicon that has a crystalline arrangement [5].

The current of electrons flowing from the drain to the source, provides enough thermal energy to disrupt the atomic structure. A uniform vibration wave due to such a disturbance is responsible for transmitting the thermal energy. Since the free medium path for the phonons is defined as the maximum propagation point for the silicon wave in SOI transistors the free medium path for the phonons is less due to the buried oxide and the miniaturization of the devices [6]. Thus, the phonon does not have its thermal energy fully consumed, since the path to be traveled is less than the path necessary for it to reach relaxation, due to such a situation the vibratory wave spreads through the material and causes the internal temperature in the transistor increase [7].

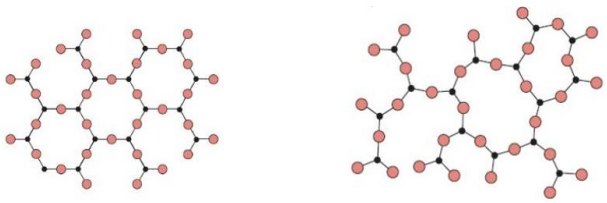

Fig. 3 - Atomic structures, the left is the crystalline arrangement, characteristic of the intrinsic silicon and the right is the amorphous arrangement, characteristic of the silicon dioxide that constitutes the buried oxide.

II. NUMERICAL SIMULATION AND ANALYSIS

Two-dimensional numerical simulations of SOI nMOSFET transistors were performed with bias different conditions and temperatures. Simulations were perfomed with and without self-heating , varying the channel length, with L= 1μm, 2μm and 3μm. Drain current as a function of drain voltage has been obtained with gate voltage overdrive (V_{GT} = $V_{GF} - V_T$, with V_{GF} being the gate voltage and V_T the threshold voltage) of 1.0 V, 2.0 V and 3.0 V. Simulations at different temperatures, ranging from 150K to 300K with 50K-step were

performed, in order to analyze the effect of temperature in the self-heating effect.

Fig. 4 shows the structure used in the numerical simulations, that were performed using Atlas software, to obtain the self-heating effect upon the drain current curves in the saturation region and upon output conductance. The simulated SOI nMOSFET features doping concentrations of $N_D=5\times10^{20}$ cm^3, $N_A=6\times10^{16}$ cm^3, with the silicon layer thickness t_{Si} = 80nm, gate oxide thickness (t_{oxf}) of 31nm, and buried oxide thickness (t_{oxb}) of 390 nm.

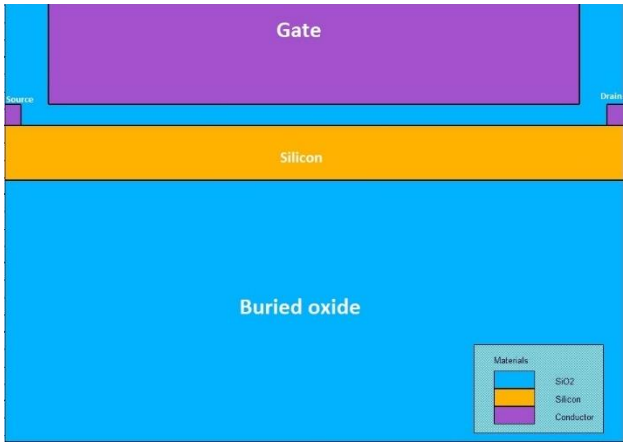

Fig. 4 - Structure of the SOI nMOSFET transistor that was used in the simulations.

III. Simulations Results

Fig. *5* shows the temperature distribution in the structure with L=1µm. One can note that due to the buried oxide the heat encounters a greater difficulty to dissipate and concentrates in the drain-channel junction. The same effect if observed in the device with L = 3µm in Fig. 6. The fact that the device has a small channel, L=1 µm, further increases self-heating. In short SOI devices self-heating is a serious problem, as current increases , the heat path through the source/drain region is squeezed and makes the temperature rise [4]. Comparing both, it can be concluded that as the device becomes shorter, larger current and smaller area for heat dissipation worsen self-heating. It can be also noted from the results in Fig. 7, that shows the lattice temperature extracted at the middle to silicon film thickness for 3 different channel lengths. One can note that the channel reaches larger temperature as the channel is shortened.

The region of the channel near the drain presents a higher temperature because it is the place with maximum electric field, so there is an increase in the drain current due to impact ionization because the generated electrons become part of the current and thus a greater self-heating effect is observed in such region [8]. In , that shows the lattice temperature extracted at the middle to silicon film thickness at different gate voltages, one can note that the higher temperature occurs near the end of the channel region. Also, as larger the gate voltage, larger drain current is obtained, resulting in higher lattice temperature.

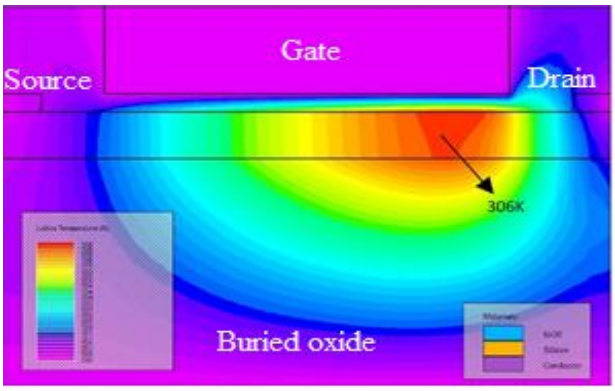

Fig. 5- Distribution of the temperature in the structure of a transistor SOI nMOSFET with a L=1µm and V_{GT} of 3.0V

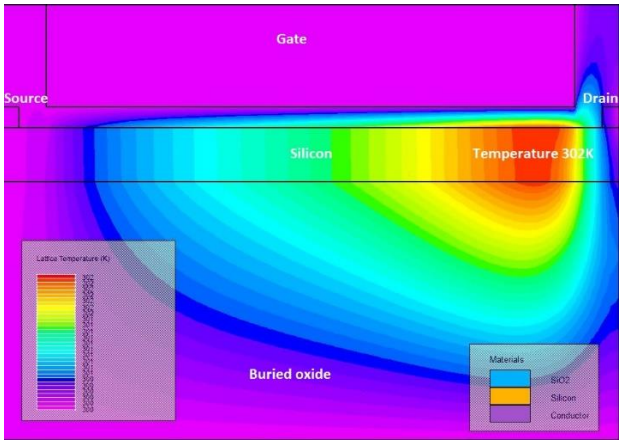

Fig. 6 - Distribution of the temperature in the structure of a transistor SOI nMOSFET with a L=3µm and VGT of 3.0V

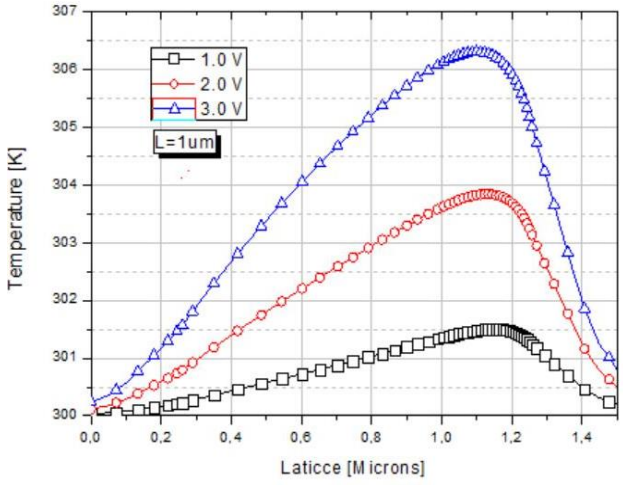

Fig. 7 - Distribution of the temperature in the silicon region for different voltages applied at the gate (VGT) and different channel length

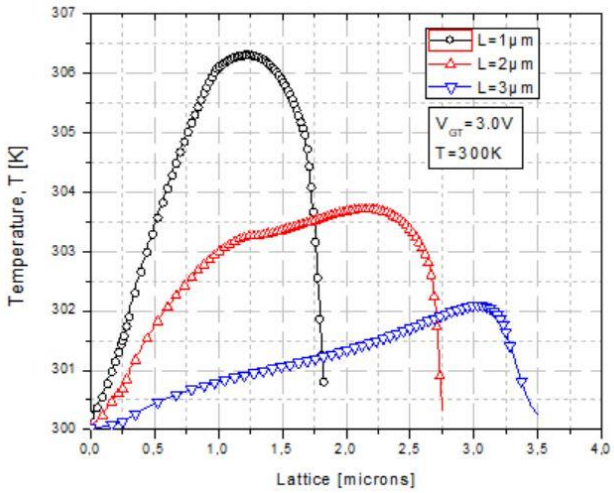

Fig. 8 - Distribution of the temperature in the silicon region for different voltages applied at the gate (VGT)

In order to simulate the self-heating effect at different temperatures, it was necessary to obtain the threshold voltage (V_T) at different temperatures, in order to adjust the gate voltage and maintain constant gate voltage overdrive. As the temperature decreases the mobility of the carriers increases due to the vibrations of the phonons decrease [9].As observed in , that shows ID vs VDS curves, as the temperature increases the mobility is degraded and so the current also suffers impact.

The increase of carriers mobility caused by temperature decrease also affects the output conductance (gD = dID/dVDS) as presented in .

Table shows the values of threshold voltage at different temperatures, extracted from I_D vs V_{GF} curves simulated at V_{DS} = 50 mV. From these results, one can note that as the temperature increases the threshold voltage tends to fall, which is in accordance with the literature.

As the temperature decreases the mobility of the carriers increases due to the vibrations of the phonons decrease [9].As observed in , that shows I_D vs V_{DS} curves, as the temperature increases the mobility is degraded and so the current also suffers impact.

The increase of carriers mobility caused by temperature decrease also affects the output conductance ($g_D = dI_D/dV_{DS}$) as presented in .

Table I - Variation of the threshold voltage due to temperature variation.

Temperature, T [K]	Threshold voltage, V_T [V]
100	0.58
150	0.54
200	0.51
250	0.46
300	0.43

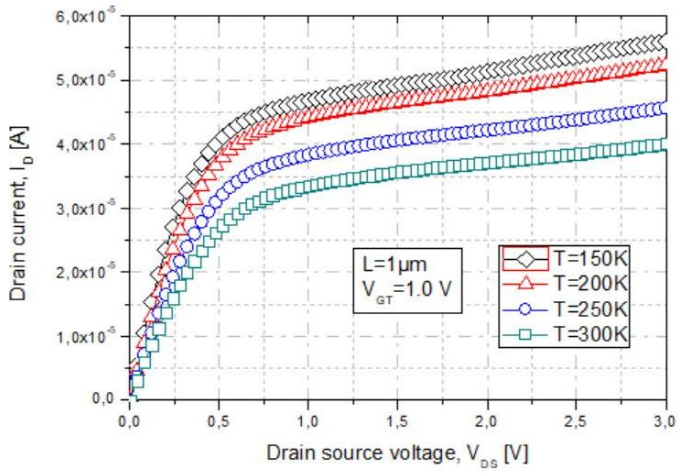

Fig. 9 - Drain current by drain voltage for different temperatures.

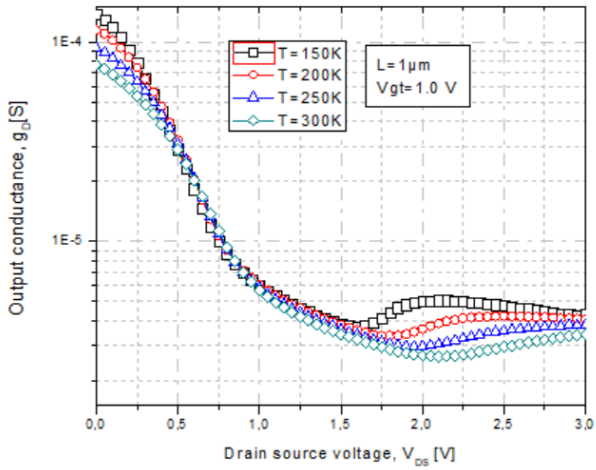

Fig. 10 - Transconductance by drain voltage for different temperatures.

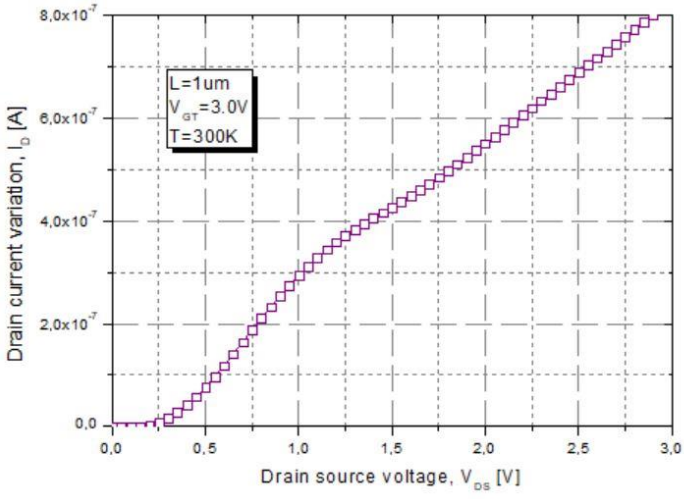

Fig. 11 - Variation of drain current due to self-heating effect.

As the gate and drain voltages increase, the current increases and self-heating effect in the transistor increases because of the difficulty in dissipating the heat. Thus the output conductance decreases, in as was presented the curve of the difference between the curves without self-heating and with self-heating.

As the temperature increases due to dissipated power (I_D x V_{DS}), thus comparing the drain current graph by the drain source voltage curves without self-heating and with self-heating, we obtain the difference curve presented in . As the curve goes into saturation the effect is becoming more pronounced and then presenting a slightly smaller current as shown in the graph above.

The higher the voltage applied to the SOI transistor gate (V_{GT}), the higher the self-heating effect because there is an increase in drain current, comparing the drain current curves in the difference between then becomes smaller due the self-heating effect.

The transconductance curves showed lower slope and a small difference between then as the gate voltage increase due to self-heating, those results can be observed in .

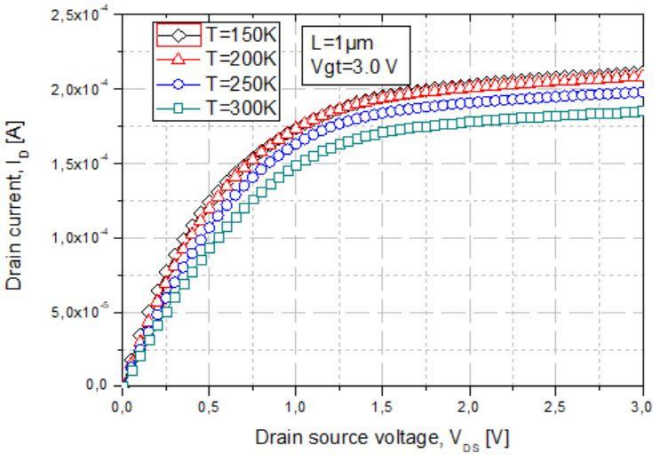

Fig. 12 - Drain current by drain voltage for different temperatures with a VGT = 3.0V

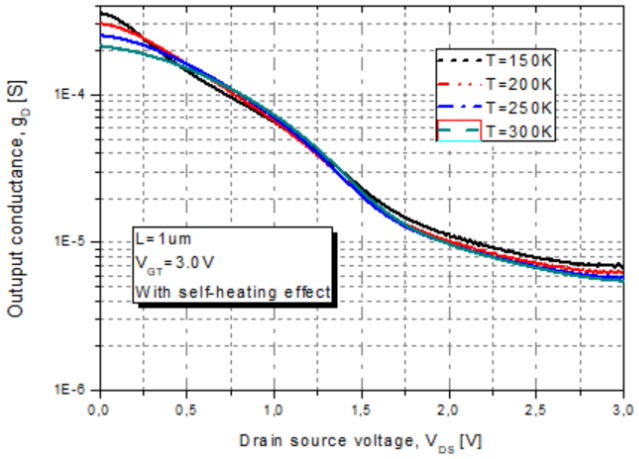

Fig. 13- Transconductance by drain voltage for different temperatures with a VGT=3.0V

IV. Conclusion

Results showed if the channel length of the SOI transistors decreases the self-heating effect will have a greater impact on the drain current as the gate voltage increases. Thus, the correct operation of short channel devices can be compromised due to the self-heating effect affecting the drain current and the conductance of the transistor.

It can also be observed in the results that as the devices become larger self-heating becomes depressible, because it impacts on the drain current are low since the heat generated is dissipated in such devices.

Acknowledgment *(Heading 5)*

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